Applicants:	DEVOR, Harold Theodore et al.	Assignee:	Intel Corporation
Serial Number:	10/721,879	Attorney Docket:	P-6216-US

REMARKS

Applicants have carefully studied the Office Action. This paper is intended to be fully responsive to all points of rejection raised by the Examiner and is believed to place the application in condition for allowance. Favorable reconsideration and allowance of the application are respectfully requested.

Status of the Claims

Claim 12 has been cancelled without prejudice to refiling in a continuation or divisional application. Claims 1, 9, 17, and 21 have been amended. Consequently, claims 1, 3-9, 11, 13-17, 19-21, and 23-32 are pending in the Application. No new matter has been added. Support for the amendments to claims 1, 9, 17, and 21 can be found in for example paragraph [0034] of the specification.

Claim Rejections Under 35 USC §103(a)

In the Office Action, the Examiner rejected claims 1, 3-7, 9, 11-15, 21, 23-26, 28-30 and 32 under 35 U.S.C. § 103(a), as being unpatentable over Hohensee et al., U.S. Patent Number 6,064,815 in view of Angel et al., U.S. Patent Number 6,643,842. Applicants respectfully traverse this rejection in view of the currently amended claims and the remarks that follow.

Claim 12 has been cancelled rendering its rejection moot.

Each of amended independent claims 1, 9, and 21 recites in paraphrase, *inter alia*, storing a location of a first memory address in a tracking list for storing the location of memory addresses for which misaligned data is detected and checking the tracking list to determine if a location of a second memory is identical to the location of the first memory address when a second instruction requires access to the second memory address. Neither of Hohensee or Angel recites these features of claims 1, 9, and 21. In particular, neither of Hohensee and Angel discloses or suggests a tracking list for storing the location of memory addresses for which misaligned data is detected and checking that tracking list with respect to the location of a second memory address.

Additionally, although the Examiner asserts that Hohensee, column 3, lines 29-35, teaches "checking if the location of a second memory address is identical...", this portion of Hohensee instead refers to the same instruction being encountered again in a loop. This is different from checking the location of a second memory address when a second instruction requires access to it, as in claims 1, 9, and 21. Angel fails to cure this deficiency of Hohensee.

Therefore, neither Hohensee nor Angel alone or in combination renders amended independent claims 1, 9, and 21 obvious.

Each of claims 3-7, 11, 13-15, 21, 23-26, 28-30 and 32 depends from one of amended independent claims 1, 9, and 21, and includes all the features of one of these amended independent claims as well as additional distinguishing features, and is therefore likewise patentable.

Furthermore, with respect to claims 29, 30, and 32, the Examiner cites Hohensee, column 3, lines 29-35 for teaching these claims. Applicants respectfully disagree. Claims 29, 30 and 32 recite in paraphrase that the location of the second memory address is identical to the location of the first memory address if the size of the difference between the first and second memory addresses is the same as the size of the data misalignment or a factor of the size of the data misalignment. The Examiner states "it's the same in this case". (Office Action, page 12). However, this portion of Hohensee refers to a loop for which the location of the second memory address is the same as the first. By contrast, claims 29, 30, and 32 have a different meaning for identical locations: "the size of the difference between the first and second memory addresses is the same as the size of the data misalignment or is a factor of the size of the data misalignment." In this instance the size of the difference is zero, not the size of the data misalignment or factor thereof. Therefore, Hohensee fails to disclose the location of the second memory address being identical to the first as the difference between the memory addresses being the same as or a factor of the data misalignment size as in claims 29, 30, and 32.

Accordingly, Applicants request that the rejection of claims 1, 3-7, 9, 11-15, 21, 23-26, 28-30 and 32 under 35 U.S.C. § 103(a), as being unpatentable over Hohensee in view of Angel be withdrawn.

The Examiner rejected claims 8, 16-17, 19-20, and 31 under 35 U.S.C. § 103(a), as being unpatentable over Hohensee in view of Angel. Applicants respectfully traverse this rejection in view of the currently amended claims and the remarks that follow.

Each of claims 8 and 16 depends from one of amended claims 1 and 9 and includes all of the features of the respective independent claim as well as additional distinguishing features. As discussed above, claims 1 and 9 are patentable over Hohensee and Angel, alone or in combination; therefore it is respectfully submitted that claims 8 and 16 are likewise patentable.

Independent claim 17 recites "to store a location of a first memory address in a tracking list for storing the location of memory addresses for which misaligned data access is detected if accessing the first memory address by a first instruction results in the misaligned data access" and "to check the tracking list to determine if a location of a second memory address is identical to the location of the first memory address when a second instruction requires access to the second memory address." Neither of Hohensee or Angel recites these features of claim 17. In particular, neither of Hohensee and Angel discloses or suggests a tracking list for storing the location of memory addresses for which misaligned data is detected and checking that tracking list with respect to the location of a second memory address. Therefore, neither Hohensee nor Angel alone or in combination renders amended independent claim 17 obvious.

Each of claims 19-20 and 31 depends from amended independent claim 17, and includes all of the features claim 17 as well as additional distinguishing features, and is therefore likewise patentable. Furthermore, for the same reasons stated above for claims 29, 30, and 32, Hohensee fails to recite the difference between the memory addresses being the same as or a factor of the data misalignment size of claim 31.

Accordingly, Applicants request that the rejection of claims 8, 16-17, 19-20, and 31 under 35 U.S.C. § 103(a), as being unpatentable over Hohensee in view of Angel be withdrawn.

The Examiner rejected claim 27 under 35 U.S.C. § 103(a), as being unpatentable over Hohensee in view of Drongowski, "Performance Tips for Alpha Linux C Programmers". Applicants respectfully traverse the rejection of Claim 27 under 35 U.S.C. § 103(a).

Claim 27 depends from amended independent claim 21; as discussed above, claim 21 is patentable over Hohensee as well as Angel. The deficiencies of Hohensee and Angel are not supplied by the teachings of Drongowski; accordingly, Applicants respectfully submit that dependent claim 27 is patentable over Hohensee and Drongowski alone, or in combination. Accordingly, the rejection of claim 27 under 35 U.S.C. § 103(a), as being unpatentable over Hohensee in view of Drongowski, is respectfully requested to be withdrawn.

Conclusion

In view of the foregoing amendment and remarks, and for at least the reasons discussed above, Applicants respectfully submit that the currently pending claims are allowable. Their favorable reconsideration and allowance are respectfully requested.

Should the Examiner have any question or comment as to the form, content or entry of this paper, the Examiner is requested to contact the undersigned at the telephone number below. Similarly, if there are any further issues yet to be resolved to advance the prosecution of this application to issue, the Examiner is requested to telephone the undersigned counsel.

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Separate from the fees for the RCE, being paid separately, no fees are believed to be due in connection with this paper. However, if any fees are due, please charge any such fees to deposit account No. 50-3355.

Respectfully submitted,

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